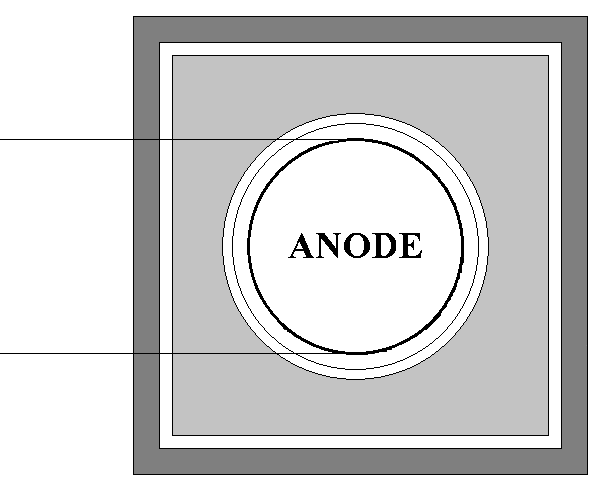
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**



**.006”**

**.015”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .006”**

**Backside Potential: Cathode**

**Mask Ref: TSS**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 8/26/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .006” P/N: 1N4148**

**DG 10.1.2**

#### Rev B, 7/19/02